## CLAIMS

1-20. (canceled)

21. (currently amended) Apparatus for a $Y$-way set-associative cache memory (e.g., 32) having $Y$>1 blocks and $X$>1 sets, wherein each block $y$, $0 \leq y \leq (Y\text{-}1)$, of each set $x$, $0 \leq x \leq (X\text{-}1)$, is adapted to store an address tag (e.g., $Tag_{xy}$), a state (e.g., $State_{xy}$), and $Z$ words (e.g., $W_{xyz}$), $0 \leq z \leq (Z\text{-}1)$, the apparatus comprising:

first circuitry (e.g., 130 and 150) adapted to (1) receive a fetch address, (2) determine a set associated with the fetch address, (3) read $Y$ address tags and $Y$ states corresponding to the associated set, (4) determine which of the $Y$ address tags are valid based on the $Y$ states, (5) compare the fetch address to one or more valid address tags, and (6) generate, if one of the valid address tags matches the fetch address, a first control signal (e.g., 110) indicating that the block associated with the matching valid address tag is a matching block;

second circuitry (e.g., 132, 138 a-d, and 134a-d) adapted to (1) receive the fetch address, (2) receive the first control signal generated by the first circuitry, (3) generate a second control signal (e.g., 126e) based on the first control signal and indicating the matching block, (4) generate block-enable control signals (e.g., 126a-d) for the cache memory, (5) apply the block-enable control signals to the cache memory, such that the matching block in the cache memory is enabled and the ($Y$-1) other blocks in the cache memory are at least partly disabled, and (6) apply the fetch address to the cache memory to read one or more associated words from the enabled matching block; and

third circuitry (e.g., 112) connected to an output of each block of the cache memory and adapted to (1) receive the second control signal generated by the second circuitry, (2) receive the one or more associated words from the enabled matching block, and (3) select the one or more associated words for output from the cache memory based on the second control signal, wherein:

the first circuitry comprises a first latch (e.g., 130) adapted to latch the fetch address;

the second circuitry comprises;

a second latch (e.g., 132) adapted to latch the first control signal and output the second control signal; and

a plurality of other latches (e.g., 134a-d) adapted to latch the block-enable control signals; and

the third circuitry comprises a multiplexer (e.g., 112) adapted to receive the outputs from the blocks and select the one or more associated words from the enabled matching block based on the second control signal from the second latch.

22. (previously presented) The invention of claim 21, wherein power consumed by each of the ($Y$-1) at least partly disabled blocks is less than power consumed by the enabled matching block.

23. (previously presented) The invention of claim 21, wherein:

during a clock cycle $k$:

the first circuitry (1) receives the fetch address, (2) determines the associated set, (3) reads the $Y$ address tags and the $Y$ states corresponding to the associated set, (4) determines the one or more valid address tags, (5) compares the fetch address to the one or more valid address tags, and (6) generates the first control signal; and

the second circuitry (1) receives the fetch address, (2) receives the first control signal, and (3) generates the block-enable control signals; and

during a next clock cycle $k$+1:

the second circuitry (1) generates the second control signal, (2) applies the block-enable control signals to the cache memory to enable the matching block and at least partly disable the ($Y$-1) other blocks and (3) applies the fetch address to the cache memory to read the one or more associated words from the enabled matching block; and

the third circuitry (1) receives the second control signal, (2) receives the one or more associated words from the enabled matching block, and (3) selects the one or more associated words for output from the cache memory based on the second control signal.

24. (canceled)

25. (currently amended) A method for operating a $Y$-way set-associative cache memory (e.g., 32) having $Y$>1 blocks and $X$>1 sets, wherein each block $y$, $0 \le y \le (Y\text{-}1)$, of each set $x$, $0 \le x \le (X\text{-}1)$, stores an address tag (e.g., $Tag_{xy}$), a state (e.g., $State_{xy}$), and $Z$ words (e.g., $W_{xyz}$), $0 \le z \le (Z\text{-}1)$, the method comprising:

(1) receiving a fetch address;

(2) determining a set associated with the fetch address;

(3) reading $Y$ address tags and $Y$ states corresponding to the associated set;

(4) determining which of the $Y$ address tags are valid based on the $Y$ states;

(5) comparing the fetch address to one or more valid address tags; and

(6) generating, if one of the valid address tags matches the fetch address, a first control signal (e.g., 110) indicating that the block associated with the matching valid address tag is a matching block;

(7) generating block-enable control signals (e.g., 126a-d) for the cache memory;

(8) generating a second control signal (e.g., 126e) based on the first control signal and indicating the matching block;

(9) applying the block-enable control signals to the cache memory, such that the matching block in the cache memory is enabled and the (*Y*-1) other blocks in the cache memory are at least partly disabled;

(10) applying the fetch address to the cache memory to read one or more associated words from the enabled matching block; and

(11) selecting the one or more associated words for output from the cache memory based on the second control signal, wherein:

step (1) comprises latching the fetch address;

step (7) comprises latching the block-enable control signals;

step (8) comprises latching the first control signal to output the second control signal; and

step (11) comprises muxing outputs from the blocks to select the one or more associated words from the enabled matching block based on the second control signal.

26. (previously presented) The invention of claim 25, wherein power consumed by each of the (*Y*-1) at least partly disabled blocks is less than power consumed by the enabled matching block.

27. (previously presented) The invention of claim 25, wherein:

a clock cycle *k* comprises (1) receiving the fetch address, (2) determining the associated set, (3) reading the *Y* address tags and the *Y* states corresponding to the associated set, (4) determining the one or more valid address tags, (5) comparing the fetch address to the one or more valid address tags, (6) generating the first control signal, and (7) generating the block-enable control signals; and

a next clock cycle *k*+1 comprises (8) generating the second control signal, (9) applying the block-enable control signals to the cache memory to enable the matching block and at least partly disable the (*Y*-1) other blocks, (10) applying the fetch address to the cache memory to read the one or more associated words from the enabled matching block, and (11) selecting the one or more associated words for output from the cache memory based on the second control signal.

28. (canceled)

29. (currently amended) A *Y*-way set-associative cache memory (e.g., 32) comprising:

$Y>1$ blocks and $X>1$ sets, wherein each block $y$, $0 \leq y \leq (Y\text{-}1)$, of each set $x$, $0 \leq x \leq (X\text{-}1)$, is adapted to store an address tag (e.g., $Tag_{xy}$), a state (e.g., $State_{xy}$), and $Z$ words (e.g., $W_{xyz}$), $0 \leq z \leq (Z\text{-}1)$;

first circuitry (e.g., 130 and 150) adapted to (1) receive a fetch address, (2) determine a set associated with the fetch address, (3) read $Y$ address tags and $Y$ states corresponding to the associated set, (4) determine which of the $Y$ address tags are valid based on the $Y$ states, (5) compare the fetch address to one or more valid address tags, and (6) generate, if one of the valid address tags matches the fetch address, a first control signal (e.g., 110) indicating that the block associated with the matching valid address tag is a matching block;

second circuitry (e.g., 132, 138 a-d, and 134a-d) adapted to (1) receive the fetch address, (2) receive the first control signal generated by the first circuitry, (3) generate a second control signal (e.g., 126e) based on the first control signal and indicating the matching block, (4) generate block-enable control signals (e.g., 126a-d) for the cache memory, (5) apply the block-enable control signals to the cache memory, such that the matching block in the cache memory is enabled and the ($Y$-1) other blocks in the cache memory are at least partly disabled, and (6) apply the fetch address to the cache memory to read one or more associated words from the enabled matching block; and

third circuitry (e.g., 112) connected to an output of each block of the cache memory and adapted to (1) receive the second control signal generated by the second circuitry, (2) receive the one or more associated words from the enabled matching block, and (3) select the one or more associated words for output from the cache memory based on the second control signal, wherein:

the first circuitry comprises a first latch (e.g., 130) adapted to latch the fetch address;

the second circuitry comprises:

a second latch (e.g., 132) adapted to latch the first control signal and output the second control signal; and

a plurality of other latches (e.g., 134a-d) adapted to latch the block-enable control signals; and

the third circuitry comprises a multiplexer (e.g., 112) adapted to receive the outputs from the blocks and select the one or more associated words from the enabled matching block based on the second control signal from the second latch.

30. (previously presented) The invention of claim 29, wherein power consumed by each of the ($Y$-1) at least partly disabled blocks is less than power consumed by the enabled matching block.

31. (previously presented) The invention of claim 29, wherein:

during a clock cycle $k$:

the first circuitry (1) receives the fetch address, (2) determines the associated set, (3) reads the *Y* address tags and the *Y* states corresponding to the associated set, (4) determines the one or more valid address tags, (5) compares the fetch address to the one or more valid address tags, and (6) generates the first control signal; and

the second circuitry (1) receives the fetch address, (2) receives the first control signal, and (3) generates the block-enable control signals; and

during a next clock cycle *k*+1:

the second circuitry (1) generates the second control signal, (2) applies the block-enable control signals to the cache memory to enable the matching block and at least partly disable the (*Y*-1) other blocks and (3) applies the fetch address to the cache memory to read the one or more associated words from the enabled matching block; and

the third circuitry (1) receives the second control signal, (2) receives the one or more associated words from the enabled matching block, and (3) selects the one or more associated words for output from the cache memory based on the second control signal.

32. (canceled)